Applicant, accordingly, respectfully requests withdrawal of the rejections of claims 18-19 and 23-25 under 35 U.S.C. § 102(e) as being anticipated by Nagy.

35 U.S.C. § 103 Rejections

The Examiner has also rejected claims 3-6, 7, 9-11, 13-15, 16, 17, 20-22, 26, and 27 under 35 U.S.C. § 103(a). Each one of these claims is either a dependent claim or has been deleted. Applicant, accordingly, respectfully withdrawal of these rejections.

SUMMARY

Applicant believes that the above remarks are fully responsive to the Office Action dated October 4, 2002. If the Examiner has any questions, Applicant respectfully requests that the Examiner contact the undersigned by telephone at (408) 720-8300.

DEPOSIT ACCOUNT AUTHORIZATION

Please charge any shortages and credit any overages to Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: November 21, 2002

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VERSION OF AMENDED SPECIFICATION AND CLAIMS WITH MARKINGS TO SHOW CHANGES

In the Specification

Page 10, Line 6:

-- Figure 1d illustrates subsequent fabrication that is carried out on the monocrystalline silicon wafer 10. First, [and] an epitaxial silicon layer 14 is grown on the monocrystalline silicon wafer 10. The epitaxial silicon layer 14 follows the crystal structure of the monocrystalline silicon wafer 10 and is thus also monocrystalline. A primary difference between the epitaxial silicon layer 14 and the monocrystalline silicon wafer 10 is that the expitaxial silicon layer 14 includes dopants. As such, the epitaxial silicon layer 14 is either n-doped or p-doped. --

Page 10, Line 13:

-- Next, integrated circuits 16A and 16B are formed. An integrated circuit 16A or 16B includes a plurality of semiconductor electronic components such as transistors, capacitors, diodes, etc., and [upper lever metalization] upper-level metallization which connect the electronic components. A transistor has source and drain regions that are implanted into the epitaxial silicon layer 14. These source and drain regions have opposite doping than the bulk of the epitaxial silicon layer 14. The source and drain regions are implanted to a required depth into the epitaxial silicon layer 14 but usually not all the way through the epitaxial silicon layer 14 so that some of the unimplanted epitaxial silicon remains below

the respective source or drain region. The metallization includes metal lines which are all located above the epitaxial silicon layer 14. Contact pads are then formed on the integrated circuits 16A and 16B. The integrated circuits 16A and 16B are identical to one another and are separated from one another by a small scribe street 18. Bumps 20 are then formed on the contact pads on the integrated circuits 16A and 16B. Although not shown, the bumps 20 are in an array and rows and columns on a respective integrated circuit 16A and 16B. --

In the Claims

Claims 3, 6, 18-24, and 28-30 have been canceled without prejudice.

1. (Amended) A wafer comprising:

a layer of solid diamond; [and]

a layer of monocrystalline semiconductor material in direct contact with the layer of solid diamond; and

a plurality of integrated circuits formed on the layer of [solid diamond] monocrystalline semiconductor material.

2. The wafer of claim 1 wherein the layer of solid diamond is at least 200 mm wide.

4. (Amended) The wafer of claim [3] 1 wherein the layer of monocrystalline semiconductor material is at least 200 mm wide.

5. (Amended) The wafer of claim [3] 1 wherein the layer of monocrystalline semiconductor material is a layer of monocrystalline silicon.

7. The wafer of claim 1 further comprising:

a plurality of contacts on the integrated circuit.

8. (Amended) A wafer comprising:

a layer of solid diamond; [and]

a final monocrystalline semiconductor film on the layer of solid diamond; and

a layer of monocrystalline semiconductor material directly on the [layer of solid diamond] final monocrystalline semiconductor film with a boundary defined between the final monocrystalline semiconductor film and the layer of monocrystalline semiconductor material for purposes of shearing the layer of monocrystalline semiconductor material from the final monocrystalline semiconductor film.

9. The wafer of claim 8 wherein the layer of solid diamond is at least 200 mm wide.

10. The wafer of claim 9 wherein the layer of monocrystalline semiconductor material is at least 200 mm wide.

11. The wafer of claim 10 wherein the layer of monocrystalline semiconductor material is a layer of monocrystalline silicon.

12. (Amended) A singulated die comprising:

a layer of solid diamond <u>having an exposed lower surface</u>; and

an integrated circuit [formed] on the layer of solid diamond.

13. (Amended) The singulated die of claim 12 further comprising:

a layer of [moncrystalline] <u>monocrystalline</u> semiconductor material on the layer of solid diamond, the integrated circuit being formed on the layer of monocrystalline semiconductor material.

14. The singulated die of claim 13 wherein the layer of monocrystalline semiconductor material is a layer of monocrystalline silicon.

15. The singulated die of claim 14 further comprising:

a layer of polysilicon on the layer of monocrystalline silicon, the layer of monocrystalline silicon being located on the layer of polysilicon.

16. The singulated die of claim 12 further comprising:

a plurality of contacts on the integrated circuit.

17. (Amended) The singulated die of claim [11] 12 wherein the die has a rectangular outline when viewed from above.

25. (Amended) [An electronic device] A wafer, comprising:

a layer of solid diamond having a thickness of less than 150 microns; and

[an] a plurality of integrated circuits [formed] in rows and columns on the layer of solid diamond.

26. (Amended) The [electronic device] wafer of claim 25 further comprising:

a layer of monocrystalline semiconductor material between the layer of diamond and the integrated circuit.

27. (Amended) The [electronic device] wafer of claim 26 wherein a layer of monocrystalline semiconductor material is a layer of [polysilicon] silicon.